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Attorney's Docket No.: 3070.1009-000

## AUTOMATIC GAIN CONTROL CIRCUIT WITH MULTIPLE INPUT SIGNALS

### RELATED APPLICATIONS

This application is related to Attorney Docket No. 3070.1008-000 entitled  
5 "Frequency Acquisition and Locking Detection Circuit for Phase Lock Loop" by  
Miao Chen Wu, *et al.*, Attorney Docket No.: 3070.1010-000 entitled "Differential Slicer  
Circuit for Data Communication", by Miao Chen Wu, and Attorney Docket No.:  
3070.1011-000 entitled "Slicer Circuit With Ping Pong Scheme For Data  
Communication", by Dev Gupta, *et al.*, filed on even date herewith. The entire  
10 teachings of the above applications are incorporated herein by reference.

### BACKGROUND OF THE INVENTION

A broadband modem typically transmits data at data rates greater than 10 Mbps  
over a coaxial cable. A cable modem can use Quadrature Amplitude Modulation  
(QAM) to obtain a high data rate. Quadrature Amplitude Modulation (QAM) is a  
15 method for doubling effective bandwidth by combining two Amplitude Modulated  
carriers in a single channel. Each of the two carriers in the channel has the same  
frequency but differs in phase by 90 degrees. One carrier is called the In-phase (I)  
signal and the other carrier is called the Quadrature (Q) signal.

A receiver receiving the QAM signal typically includes an amplifier with  
20 Automatic Gain Control (AGC) circuitry. The AGC circuitry senses the peak to peak  
voltage at the output of the amplifier and adjusts the gain of the amplifier so that the

peak to peak voltage is constant regardless of the peak to peak voltage of the received QAM signal.

In operation, the amplifier's output signal is peak-detected to provide a D.C. voltage. The D.C. voltage is amplified and used to control the gain of the amplifier.

- 5 The D.C. voltage is proportional to the received QAM signal. Thus, the greater the peak to peak voltage of the received QAM signal, the greater the D.C. voltage. Increasing the D.C. voltage reduces the gain of the amplifier.

- 10 An Automatic Gain Control Circuit typically compares the D.C. voltage corresponding to the peak to peak voltage of the I carrier in the received QAM signal with a reference D.C. voltage level in a differential amplifier. The D.C. voltage level on the output of the differential amplifier is an indication of whether the gain should be increased or decreased.

#### SUMMARY OF THE INVENTION

- 15 It is difficult to set the proper AGC gain before the carriers are recovered by the receiver. However, without the proper AGC gain, it is hard to recover the carriers.

- According to the present approach, information from an estimated amplitude signal or a recovered carrier is used to set the gain of the AGC. A first peak detector detects a signal peak voltage from an estimated amplitude signal or from a carrier signal recovered from a received signal. An integrator sets the gain dependent on a difference  
20 between the peak signal voltage and a peak reference voltage.

- A converter converts the estimated amplitude signal, the recovered carrier signal and a reference signal to a same common mode. The first peak detector detects the signal peak voltage from the estimated amplitude signal and the converted recovered carrier signal. A second peak detector detects the peak reference voltage from the  
25 converted reference signal.

The peak signal voltage is detected from the estimated amplitude signal until the amplitude of the carrier signal decreases below the amplitude of the estimated amplitude signal. The peak signal is detected from the I signal after the carrier is recovered.

In one embodiment the carrier signal is an I signal. In alternate embodiments, the carrier signal can be a Q signal or include an I signal and a Q signal.

#### BRIEF DESCRIPTION OF THE DRAWINGS

5       The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the  
10   invention.

Fig. 1 illustrates an embodiment of a network configuration of intelligent network elements for providing point to point data links between intelligent network elements in a broadband, bidirectional access system.

Fig. 2 is a block diagram of an embodiment of any one of the network elements  
15   shown in Fig. 1.

Fig. 3 is a diagram of a frame structure for use in the network of Fig. 1;

Fig. 4 is a block diagram of a receiver in any of the modems in the network element shown in Fig. 2.

Fig. 5A is a block diagram of an Automatic Gain Control (AGC) circuit in the  
20   receiver shown in Fig. 4 according to the principles of the present invention;

Fig. 5B is a circuit diagram of the threshold voltage circuit supplying the reference voltages to the AGC circuit shown in Fig. 5A.

Fig. 6A is a graph illustrating the non-linear relationship between the estimated amplitude signal and the recovered I (or Q) signal;

25       Fig. 6B is a signal diagram illustrating the relationship between the estimated amplitude signal and the recovered I signal;

Fig. 7A is a block diagram of an embodiment of an estimated amplitude signal generation circuit in the SYNC timing circuit 472 shown in Fig. 3;

Fig. 7B is a circuit diagram of the differential amplifiers and biasing circuit shown in Fig. 5A; and

Fig. 8 is a circuit diagram of the peak detectors shown in Fig. 5A.

#### DETAILED DESCRIPTION OF THE INVENTION

5 A description of preferred embodiments of the invention follows.

Fig. 1 illustrates an embodiment of a network configuration of intelligent network elements for providing point to point data links between intelligent network elements in a broadband, bidirectional access system. This network configuration is described in U.S. Patent Application No. 09/952,321 filed September 13, 2001 entitled  
10 "Broadband System With Topology Discovery", by Gautam Desai, *et al*, the entire teachings of which are incorporated herein by reference. The network configuration, also referred to herein as an Access Network, includes intelligent network elements each of which uses a physical layer technology that allows data connections to be carried over coax cable distribution facilities from every subscriber. In particular, point-to-point data  
15 links are established between the intelligent network elements over the coax cable plant. Signals are terminated at the intelligent network elements, switched and regenerated for transmission across upstream or downstream data links as needed to connect a home to the headend.

The intelligent network elements are interconnected using the existing cable  
20 television network such that the point-to-point data links are carried on the cable plant using bandwidth that resides above the standard upstream/downstream spectrum. For example, the bandwidth can reside at 1025 to 1125 MHZ (upstream) and 1300 to 1400 MHZ (downstream) or 100 Mbps upstream and downstream bandwidths can be provided in the spectrum 750 to 860 MHZ or duplexing channel spectrums can be  
25 allocated in the 777.5MHz to 922.5MHz regime for 100Mb/s operation and in the 1 GHz to 2GHz regime for 1Gb/s operation.

The intelligent network elements include an intelligent optical network unit or node 112, intelligent trunk amplifier 114, intelligent tap or subscriber access switch

(SAS) 116, intelligent line extender 118 and network interface unit (NIU) 119. A standard residential gateway or local area network 30 connected to the NIU 119 at the home is also shown. Note that the trunk amplifier 114 is also referred to herein as a distribution switch (DS). The configuration shown includes ONU assembly 312  
5 comprising standard ONU 12 and intelligent ONU 112 also referred to herein as an optical distribution switch (ODS). Likewise, trunk amplifier or DA assembly 314 includes conventional trunk amp 14 and intelligent trunk amp 114; cable tap assembly 316 includes standard tap 16 and subscriber access switch 116; and line extender assembly 318 includes standard line extender 18 and intelligent line extender 118.

10 The intelligent ONU or ODS is connected over line 15 to a router 110, which has connections to a server farm 130, a video server 138, a call agent 140 and IP network 142. The server farm 130 includes a Tag/Topology server 132, a network management system (NMS) server 134, a provisioning server 135 and a connection admission control (CAC) server 136, all coupled to an Ethernet bus which are described  
15 in U.S. Patent Application No. 09/952,321 filed September 13, 2001 entitled "Broadband System With Topology Discovery", by Gautam Desai, *et al*, the entire teachings of which are incorporated herein by reference.

A headend 10 is shown having connections to a satellite dish 144 and CMTS 146. To serve the legacy portion of the network, the headend 10 delivers a conventional  
20 amplitude modulated optical signal to the ONU 12. This signal includes the analog video and DOCSIS channels. The ONU performs an optical to electrical (O/E) conversion and sends radio frequency (RF) signals over feeder coax cables 20 to the trunk amplifiers or DAs 14. Each DA along the path amplifies these RF signals and distributes them over the distribution portion 24.

25 The present system includes intelligent network elements that can provide high bandwidth capacity to each home. In the Access Network of the present invention, each intelligent network element provides switching of data packets for data flow downstream and statistical multiplexing and priority queuing for data flow upstream. The legacy video and DOCSIS data signals can flow through transparently because the

intelligent network elements use a part of the frequency spectrum of the coax cable that does not overlap with the spectrum being used for legacy services.

Fig. 2 is a block diagram of an embodiment of any one of the network elements shown in Fig. 1. The network element includes an RF complex 202, RF  
 5 transmitter/receiver pairs or modems 204a-204n, a PHY (physical layer) device 206, a switch 208, microprocessor 210, memory 212, flash memory 217 and a local oscillator/phase locked loop (LO/PLL) 214. All of the components are common to embodiments of the ODS, DS, SAS and NIU shown in Fig. 1. The ODS further includes an optical/electrical interface. The NIU further includes a 100BaseT physical  
 10 interface for connecting to the Home LAN 30 (FIG. 2). In addition, the RF complex is shown as having a bypass path 218A and a built in self test path 218B controlled by switches 218C, 218D which are described further herein.

The number of modems, 204n generally, depends on the number of links that connect to the network element. For example, DS 314 (Fig. 1) has five ports and thus  
 15 has five modems 204. A SAS 316 (Fig. 1) has six ports and thus has six modems 204. The network element in Fig. 2 is shown having six ports indicated as ports 203, 205, 207, 209, 211 and 213.

The PHY device 206 provides physical layer functions between each of the modems 204 and the switch 208. The switch 208, controlled by the microprocessor  
 20 210, provides layer 2 switching functions and is referred to herein as the Media Access Control ("MAC") device or simply MAC. The LO/PLL 214 provides master clock signals to the modems 204 at the channel frequencies.

A modulation system with spectral efficiency of 4 bits/s/Hz is used in the RF modem 604n (Fig. 2) to provide high data rates within the allocated bandwidth. In  
 25 particular, 16-state Quadrature Amplitude Modulation (16-QAM) is preferably used, which involves the quadrature multiplexing of two 4-level symbol channels. Embodiments of the network elements of the present system described herein support 100 Mb/s and 1 Gb/s Ethernet transfer rates, using the 16-QAM modulation at symbol rates of 31 or 311 MHZ.

Fig. 3 is a block diagram of a frame structure 320 for use in the network of Fig.

1. The frame structure 320 is used to transmit a frame over the network. The frame structure 320 includes frame synchronization 300, symbol synchronization 302 and a data phase 304. In a particular embodiment, frame and symbol synchronization is
- 5 performed every 10 micro seconds ( $\mu\text{s}$ ) followed by 1280 bytes of Data Phase 621, with frame synchronization (FS) 300 for  $1\mu\text{s}$  and the symbol synchronization (SS) 302 for 400 nano seconds (ns). It should be understood that other frame structures are possible and the frame structure described is only an example.

- Fig. 4 is a block diagram of a receiver 204B in any of the modems 204 in the
- 10 network element shown in Fig. 2. The receiver 204B receives a quadrature-multiplexed signal which includes in-phase (I) and quadrature (Q) carriers. At the front end, the receiver section 204B includes low-noise amplifier (LNA) 450, equalizer 452 and automatic gain control (AGC) 454. The received signal from PHY 206 (Fig. 2) is boosted in the LNA 450 and corrected for frequency-dependent line loss in the equalizer
  - 15 452. The equalized signal is passed through the AGC stage 454 to I and Q multiplier stages 456, 458, low pass filters 460 and analog-to-digital converters (ADC) 462. After down-conversion in the multiplier stages 456, 458 and low-pass filtering, the I and Q channels are digitized and passed on to the QAM-to-byte mapper 429 for conversion to a byte-wide data stream in the PHY device 406 (Fig. 2).

- 20 Carrier and clock recovery, for use in synchronization at symbol and frame levels, are performed during periodic training periods. A carrier recovery PLL circuit 468 provides the I and Q carriers from the RF carrier (RFin) 520 to the multipliers 456, 458. The RF carrier 520 includes the I and Q carriers. A clock recovery delay locked loop (DLL) circuit 476 provides a clock to the QAM-to-byte mapper 449. During each
- 25 training period, PLL and DLL paths that include F(s) block 474 and voltage controlled oscillator (VCXO) 470 are switched in using normally open switch 473 under control of SYNC timing circuit 472 in order to provide updated samples of phase/delay error correction information.

The AGC stage 454 amplifies the equalized signal to output an amplified signal with a constant peak to peak voltage. In one embodiment the gain of the AGC stage 454 is selected to output an amplified signal with a peak to peak voltage of 300 milli Volts (mV).

5 Fig. 5A is a block diagram of the Automatic Gain Control (AGC) stage 454 in the receiver 204B shown in Fig. 4 according to the principles of the present invention. The AGC stage 454 includes differential amplifiers 508, 510, 512, peak detectors 500, 502, an integrator 504 and an RF Variable Gain Amplifier (VGA) 506. An estimated amplitude signal ( $I^2 + Q^2$ ) from the SYNC timing circuit 472 (Fig. 3) and the I signal  
10 from low pass filters 460 (Fig. 3) are input to the AGC stage 454.

Each of the differential amplifiers 508, 510, 512 is open loop; that is, there is nothing coupled between the inputs and the outputs. In theory, an ideal open loop differential amplifier rejects any common mode voltage when there is no differential input voltage; that is, the voltage level on both inputs is the same. The ideal open loop  
15 differential amplifier outputs a differential voltage of 0 V when there is no differential input voltage. In practice, even with no differential input voltage, there is a small differential output voltage which is dependent on the open loop common-mode gain of the differential amplifier. To minimize the effect of different open-loop common mode gain in each of the differential amplifiers, the same biasing voltage and same  
20 degeneration resistor are applied to each differential amplifier 508, 510, 512 by the biasing circuit 518. Also, the components in each of the differential amplifiers are selected so that the differential amplifiers are matched to minimize the difference in the common mode voltage.

By applying the same biasing voltage and with same degeneration resistor to  
25 each differential amplifier 508, 510, 512, a differential estimated amplitude signal, I signal and reference signal are converted to a converted differential estimated amplitude signal, converted I signal and converted reference signal having the same common mode voltage. The converted signals output from the differential amplifiers 508, 510, 512 are coupled to peak detectors 500, 502.



Converted differential  $I^2 + Q^2$  signal and converted I signal are coupled to peak detector 500. A converted reference signal 508 dependent on a differential reference voltage  $R_{in+}$ ,  $R_{in-}$  output by the ADC 462 (Fig. 4) is coupled to peak detector 502. The reference voltage  $R_{in+}$ ,  $R_{in-}$  is output by the same reference voltage circuit

5 outputting the reference voltages for a slicer circuit in the ADC 462 (Fig. 4) so that the incoming I and Q signal magnitude controlled by the AGC tracks the slicer reference. The slicer circuit is described in co-pending U.S. Patent Application Attorney Docket No. 3070-1010-00 entitled "Differential Slicer Circuit for Data Communication" by Miao Chen Wu, the entire teachings of which are incorporated herein by reference. Each

10 peak detector detects the peak voltage on the input signal and outputs the detected peak voltage on an output signal. The peak detector typically includes a capacitor. While the input voltage is greater than the previously detected peak voltage, the capacitor charges up to the input voltage. While the input voltage is less than the previously detected peak voltage, the peak detector maintains the output voltage at the previously detected peak

15 voltage level.

Peak detector 500 outputs the signal peak voltage detected on either the converted estimated amplitude signal or the converted I signal on the peak signal 514. Peak detector 502 outputs the reference peak voltage 516. The difference between the signal peak 514 and the reference peak 502 represents the amplitude difference between

20 the incoming signals ( $I^2 + Q^2$ , and I) and the reference signal. The difference is integrated through an integrator 504. The output of the integrator controls the Variable Gain Amplifier (VGA) 506 to set the AGC gain for amplifying the equalized signal.

The converted differential signal for the estimated amplitude signal generates the peak signal 514 in peak detector 500. The peak signal 514 is dependent on whether the

25 peak voltage is detected on the estimated amplitude signal or the I signal. Initially, the amplitude of the estimated amplitude signal is larger and the peak voltage detected is used to estimate the AGC gain. After the I signal is recovered, the peak voltage is detected from the I signal because the amplitude of the I signal is greater than the amplitude of the estimated amplitude signal. As the amplitude of the converted

differential signal for the estimated amplitude signal decreases below the amplitude of the I signal, the peak signal 514 detected from the I signal fine tunes and maintains the AGC gain after the I signal is recovered.

Fig. 5B is a circuit diagram of the threshold voltage circuit supplying the  
 5 reference voltages to the AGC circuit shown in Fig. 5A. The reference voltage  $R_{in}^+$ ,  $R_{in}^-$  coupled to differential amplifier 512 (Fig. 5A) is output by the same threshold voltage circuit supplying the reference voltages to the AGC circuit so that the incoming I and Q signals match and track the slicer reference.

The threshold voltage circuit includes a bandgap reference 530, a buffer 532 and  
 10 resistors 534, 536, 538. The voltage level of threshold voltages  $V_{ref}^+$ ,  $V_{ref}^-$  and  $R_{in}^+$ ,  $R_{in}^-$  are dependent on the voltage level on the output of buffer 514 and the resistance values of resistors 534, 536, 538.  $V_{REF}^+$ ,  $V_{REF}^-$  are coupled to the ADC 462.  $R_{in}^-$  is the same reference voltage as the  $V_{REF}^-$ . Thus  $R_{in}^+$ ,  $R_{in}^-$  tracks the slicer reference  $V_{REF}^+$ ,  $V_{REF}^-$ .

Fig. 6A is a graph illustrating the non-linear relationship between the estimated  
 15 amplitude signal and the recovered I (or Q) signal. There is a non-linear relationship between the amplitude of the  $I^2 + Q^2$  and the I signal as the amplitude of the signals decreases when the carriers are recovered. The graph shows  $A^2(x)$  and  $A(x)$ .  $A(x)$  corresponds to the function  $y = x$ .  $A(x)$  is a linear function, for example, for  $x = 0.1$ ,  
 20  $0.2, 0.3, \dots, 1, 2, 3$ ,  $A(x) = 0.1, 0.2, 0.3, \dots, 1, 2, 3$  because  $y = x$ .  $A^2(x)$  is a non-linear function, for example, for  $x = 0.1, 0.2, 0.3, \dots, 1, 2, 3$ ,  $A^2(x) = 0.01, 0.04, 0.09, \dots, 1, 4.9$  because  $y = x^2$ . Thus for values of  $x$  greater than 1,  $A(x)$  is less than  $A^2(x)$  and for values of  $x$  less than 1  $A(x)$  is greater than  $A^2(x)$ .

Fig. 6B is a signal diagram illustrating the relationship between the estimated  
 25 amplitude signal and the recovered I (or Q) signal. At time  $t_1$  before the carrier is recovered,  $x$  is 2 and the amplitude of the estimated amplitude signal ( $I^2 + Q^2$ ) is 4 ( $x^2$ ) which is greater than 2 ( $x$ ), the amplitude of the I signal. Thus, the peak voltage is detected from the  $I^2 + Q^2$  signal. At time  $t_2$ , the carrier is recovered,  $x = 1$  and the amplitude of the  $I^2 + Q^2$  signal and the I signal is equal. Thus, the peak voltage can

be detected from either the  $I^2 + Q^2$  signal or the I signal. At time  $t_3$ , the amplitude of the I signal is greater than that of the  $I^2 + Q^2$  signal with  $x = 0.8$  and  $x^2 = .64$ .

Thus, the peak voltage is detected from the I signal.

Fig. 7A is a block diagram of an embodiment of an estimated amplitude signal generation circuit in the SYNC timing circuit 472 shown in Fig. 4. The amplitude of the estimated amplitude signal provides an estimate for the AGC gain until the I and Q signals are recovered. The estimated amplitude signal is used to estimate the AGC gain because the estimated amplitude signal is independent of the I and Q signal recovery a D.C. signal.

In theory, the estimated amplitude signal is a signal related only to I and Q signals which can be a D.C. signal. The estimated amplitude signal is derived as follows: The I signal can be represented as  $A \cos \omega t$ . The Q signal is  $90^\circ$  out of phase with the I signal and can be represented as  $A \sin \omega t$ . Summing the square of the I signal and the square of the Q signal results in a signal that can be represented as  $A^2 \cos^2 \omega t + A^2 \sin^2 \omega t$ . Replacing for  $\cos^2 \omega t + \sin^2 \omega t = 1$ , results in a signal with a voltage of amplitude  $A^2$ . A is a function of time.

In one embodiment, the AGC gain is selected to output an amplified signal with a peak to peak voltage of 300 milli Volts (mV). The I signal 600 is squared in multiplier 604. The Q signal 602 is squared in multiplier 606. A squared I signal  $I^2$  is output by multiplier 604 and a squared Q signal  $Q^2$  is output by multiplier 606. The  $I^2$  and  $Q^2$  signals are summed in adder 608. Adder 608 outputs the estimated amplitude signal, that is, a signal of amplitude  $A^2$ .

Fine tuning of the ACG gain is performed after the I and Q signals are recovered by the I signal, Q signal or both. The estimated amplitude signal cannot be used to fine tune the AGC gain because the amplitude of the estimated amplitude signal changes dependent on temperature and power supply voltages, and it has nonlinear relationship with the I and Q signals. After the I signal and Q signal are recovered, the amplitude of the estimated amplitude signal decreases faster than the I signal and Q signal, thereby allowing the I signal to generate the peak signal 514 in peak detector 500.

Fig. 7B is a circuit diagram of the differential amplifiers 508, 510, 512 and the biasing circuit 518 shown in Fig. 5A. The biasing circuit 518 injects a biasing voltage to each differential amplifier 508, 510, 512. The biasing voltage is injected to differential amplifier 508 through transistor 840, to differential amplifier 510 through transistor 842 and to differential amplifier 512 through transistor 843. The circuit for injecting the common mode voltage is the same for all the differential amplifiers 508, 510, 512 and will be described for differential amplifier 508.

Differential amplifier 508 includes transistors 800, 802 and resistors 812, 814, 816, 818. The common mode output voltage is dependent on the voltage level injected from the biasing circuit 518 between resistors 816, 818 and resistors 812, 814 which are common to all the differential amplifiers 508, 510, 512. When there is a common mode input on  $(I^2 + Q^2)^+_{OUT}$ ,  $(I^2 + Q^2)^-_{OUT}$ , that is, the same signal is applied to  $(I^2 + Q^2)^+_{OUT}$  and  $(I^2 + Q^2)^-_{OUT}$  and there is no differential input voltage, if each side of the differential amplifier is identical, the differential output voltage will be about zero volts.

Fig. 8 is a block diagram of peak detectors 500 and 502 shown in Fig. 5A. Peak detector 502 generates the peak reference signal 516 and includes transistor 704 and capacitor 706. The emitter of transistor 704 is coupled to capacitor 706 and to peak reference signal 516. Transistor 704 is turned 'on' and an emitter current flows when the voltage level on the reference signal  $R_{OUT}^+$  coupled to the base of transistor 704 is greater than the voltage level on the peak reference signal 516 coupled to the emitter of transistor 704. While transistor 704 is 'on', current flows through capacitor 706 and capacitor 706 charges up to the voltage level at the emitter of the transistor 704.

When the voltage level on the reference signal  $R_{OUT}^+$  coupled to the base of transistor 704 decreases below the voltage level on the peak reference signal 516, transistor 704 turn 'off' and acts like an open circuit maintaining the peak reference signal 516 at the current peak reference voltage level. Transistor 704 is turned 'on' again when the voltage level on the converted reference signal increases above the

current peak reference voltage on the peak reference signal 516. As the reference signal  $R_{OUT}$  is constantly unchanged, the capacitor 706 holds the voltage all the time.

Peak detector 500 includes transistors 708, 710, 712, 714 and capacitor 716. The emitters of each of the transistors 708, 710, 712, 714 are coupled together and to capacitor 716. While any one of transistors 708, 710, 712, 714 is 'on', capacitor 716 charges to the voltage level at the emitter of the respective transistor 708, 710, 712, 714.

Thus, a differential voltage on the  $I^2 + Q^2$  signal or on the I signal greater than the current peak voltage level on the signal peak signal 514 turns the respective transistor 708, 710, 712, 714 'on' to charge up capacitor 716 to the peak signal voltage. Therefore, the voltage on the peak signal 516 is the peak signal voltage detected on either the  $I^2 + I^2Q$  signal or the I signal. Before the I signal is recovered, the  $I^2 + Q^2$  differential signal 708, 710 generates the peak signal voltage 514 to provide an estimated value for the AGC gain. As discussed in conjunction with Fig. 6A, there is a non-linear relationship between the amplitude of the  $I^2 + I^2$  signal and the I signal. After the I signal is recovered, the amplitude of the  $I^2 + Q^2$  signal decreases much faster than the amplitude of the I signal. Thus, after the I signal is recovered, the I signal generates the peak signal voltage 514 to fine tune and maintain the AGC gain.

Before the I signal and Q signal are recovered, a differential voltage on the  $(I^2 + Q^2)^+_{OUT}$  signal greater than the peak signal voltage 514 results in an emitter current in transistor 708. The amount of the emitter current is dependent on the voltage at the base of transistor 708. Capacitor 716 charges while there is an emitter current. Similarly, a negative differential voltage on the  $(I^2 + Q^2)^-_{OUT}$  signal greater than the peak signal voltage 514 results in an emitter current in transistor 710. Capacitor 716 charges dependent on the emitter current. While the transistor is 'off' the base-emitter junction is reversed biased to maintain the detected peak voltage.

After the I signal is recovered, the peak signal voltage 514 is controlled by the I signal as the amplitude of the  $I^2 + Q^2$  signal decreases below the amplitude of the I signal. Transistor 712 is turned 'on' by a positive differential voltage  $I^+_{OUT}$  greater than

the peak signal voltage 514 and transistor 714 turned 'on' by a negative differential voltage  $I_{OUT}$  greater than the peak signal voltage 514.

In the embodiment shown, the peak signal voltage 514 is the peak voltage detected on either the  $I^2 + Q^2$  signal or the I signal. In an alternative embodiment, the I signal can be replaced by the Q signal or another pair of transistors can be added to the peak detector 500 to also detect the peak voltage on the Q signal. The addition of the transistors to the peak detector 500 to also detect the peak voltage on the Q signal increases the accuracy of the AGC gain.

Transistor 718 in peak detector 502 provides a bias current to maintain the reference peak voltage 516. The bias current is small when the peak detection transistors are 'off', typically on the order of 1 nano Amp (nA) to limit the leakage current. Similarly, transistors 720, 722, 724, 726 in peak detector 500 provide a bias current for the signal peak voltage 514.

The voltage levels on the peak signal voltage 514 and the peak reference signal 516 are dependent on the current supplied to the capacitors 706, 716, the capacitance of the capacitors 706, 716 and the charging time. For example, if a current  $I(t)$  is applied at time  $t = 0$ , then the voltage at time  $t$  can be computed using the following equation:

$$V(t) = V_0 + \int_0^t \frac{I}{C} dt \quad t \geq 0$$

where  $V_0$  is the initial voltage at  $t = 0$ ; and

C is the capacitance of the capacitor.

Thus, the respective bias current through the respective capacitor 706, 716 maintains the respective peak voltage 514, 516. Using the estimated amplitude signal to estimate the AGC gain before the I signal and Q signal are recovered allows recovery of the I signal and Q signal. Thus, the AGC gain is estimated in order to recover the carriers, and after the carriers are recovered, the AGC gain is accurately set by one or more of the recovered carriers.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

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